UNNAMALAI INSTITUTE OF TECHNOLOGY

Suba Nagar, Kovilpatti–628502

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

An ISO 9001:2015 Certified Institution

Department of Computer Science and Engineering

VCSE2201 Designing of Digital System Using VHDL

Assessment Question and Answer

Name :

Register No :

Year/Department :

No of Question: 20	Mark: 20	Duration: 30mins

1) What is the full form of EDA in terms of VHDL?

A. Electronic Design Automation

B. Electrical Data Automation

C. Electronic Data Auto-collection

D. Electrical Design Adapter

2) The act of building a model or representation of a digital circuit or system in order to forecast its behaviour and evaluate its usefulness is known as ____.

A. Implementation

B. Simulation

C. Verification

D. Synthesis

3) The process of validating that a digital design satisfies its functional a and performance criteria is referred to as ____.

A. Implementation

B. Simulation

C. Verification

D. Synthesis

4) The process of converting a high-level hardware description language (HDL) design, such as VHDL, into a lower-level representation, often a gate-level netlist, is known as ____.

A. Implementation

B. Simulation

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

C. Verification

D. Synthesis

5) Port name in VHDL is

A. Case sensitive

B. Case insensitive

6) VHDL code is converted into a gate-level representation or netlist by which of the following tools?

A. Verification tools

B. Place and route tools

C. Time analysis tools

D. Synthesis tools

7) Which of the following is not an example of a synthesis tool?

A. Yosys

B. Cadence Genus

C. Prime time

D. Xilinx Vivado HLS

8) Is there any visual or graphical information in a net list file?

A. Yes

B. No

9) Does HDLs emphasize the concept of abstraction?

A. Yes

B. No

10) An HDL takes which of the following approaches?

A. Structure and behavioural approach

B. Object-oriented approach

C. Master-servant approach

11) Verilog enables which modelling techniques?

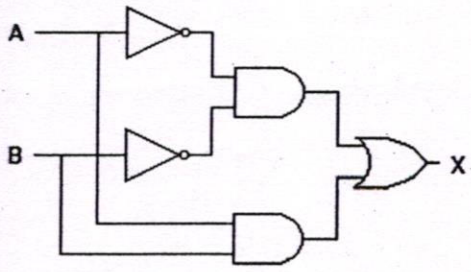
A. Structural modelling techniques

B. Behavioural modelling techniques

C. Both

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

12) What type of logic circuit is represented by the figure shown below?



a) XOR

b) XNOR

c) AND

d) XAND

13) Which of the following combinations of logic gates can decode binary 1101?

a) One 4-input AND gate

b) **One 4-input AND gate, one inverter**

c) One 4-input AND gate, one OR gate

d) One 4-input NAND gate, one inverter

14) What is the indication of a short to ground in the output of a driving gate?

a) Only the output of the defective gate is affected

b) There is a signal loss to all load gates

c) The node may be stuck in either the HIGH or the LOW state

d) The affected node will be stuck in the HIGH state

14) The carry propagation can be expressed as _____

a) Cp = AB

b) Cp = A + B

c) All but Y0 are LOW

d) All but Y0 are HIGH

15) 3 bits full adder contains _____

a) 3 combinational inputs

b) 4 combinational inputs

c) 6 combinational inputs

d) **8 combinational inputs**

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

16) Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?

a. Simulation

b. Optimization

c. Synthesis

d. Verification

17) In VLSI design, which process deals with the determination of resistance & capacitance of interconnections?

a. Floor planning

b. Placement & Routing

c. Testing

d. Extraction

18) In VHDL, which object/s is/are used to connect entities together for the model formation?

a. Constant

b. Variable

c. Signal

d. All of the above

19) Which data type in VHDL is non synthesizable & allows the designer to model the objects of dynamic nature?

a. Scalar

b. Access

c. Composite

d. File

20) Which type of simulation mode is used to check the timing performance of a design?

a. Behavioural

b. Switch-level

c. Transistor-level

d. Gate-leve

Course Coordinator **HoD**

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

UNNAMALAI INSTITUTE OF TECHNOLOGY

Suba Nagar, Kovilpatti–628502

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

An ISO 9001:2015 Certified Institution

Department of Computer Science and Engineering

VCSE2201 Designing of Digital System Using VHDL

Assessment Question and Answer

20/20

Name : K. Mesack

Register No : 953119104015

Year/Department : IV / CSE

No of Question: 20	Mark: 20	Duration: 30mins

1) What is the full form of EDA in terms of VHDL?

A. Electronic Design Automation

B. Electrical Data Automation

C. Electronic Data Auto-collection

D. Electrical Design Adapter

2) The act of building a model or representation of a digital circuit or system in order to forecast its behaviour and evaluate its usefulness is known as ____.

A. Implementation

B. Simulation

C. Verification

D. Synthesis

3) The process of validating that a digital design satisfies its functional a and performance criteria is referred to as ____.

A. Implementation

B. Simulation

C. Verification

D. Synthesis

4) The process of converting a high-level hardware description language (HDL) design, such as VHDL, into a lower-level representation, often a gate-level netlist, is known as ____.

A. Implementation

B. Simulation

C. Verification

D. Synthesis

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

5) Port name in VHDL is

A. Case sensitive

B. Case insensitive

6) VHDL code is converted into a gate-level representation or netlist by which of the following tools?

A. Verification tools

B. Place and route tools

C. Time analysis tools

D. Synthesis tools

7) Which of the following is not an example of a synthesis tool?

A. Yosys

B. Cadence Genus

C. Prime time

D. Xilinx Vivado HLS

8) Is there any visual or graphical information in a net list file?

A. Yes

B. No

9) Does HDLs emphasize the concept of abstraction?

A. Yes

B. No

10) An HDL takes which of the following approaches?

A. Structure and behavioural approach

B. Object-oriented approach

C. Master-servant approach

11) Verilog enables which modelling techniques?

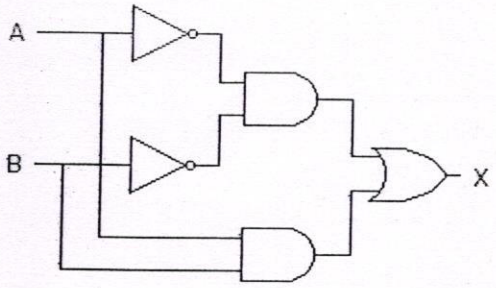
A. Structural modelling techniques

B. Behavioural modelling techniques

C. Both

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

12) What type of logic circuit is represented by the figure shown below?



a) XOR

b) XNOR

c) AND

d) XAND

13) Which of the following combinations of logic gates can decode binary 1101?

a) One 4-input AND gate

b) One 4-input AND gate, one inverter

c) One 4-input AND gate, one OR gate

d) One 4-input NAND gate, one inverter

14) What is the indication of a short to ground in the output of a driving gate?

a) Only the output of the defective gate is affected

b) There is a signal loss to all load gates

c) The node may be stuck in either the HIGH or the LOW state

d) The affected node will be stuck in the HIGH state

14) The carry propagation can be expressed as _____

a) Cp = AB

b) Cp = A + B

c) All but Y0 are LOW

d) All but Y0 are HIGH

15) 3 bits full adder contains _____

a) 3 combinational inputs

b) 4 combinational inputs

c) 6 combinational inputs

d) 8 combinational inputs

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

16) Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?

a. Simulation
b. Optimization
c. Synthesis
d. Verification

17) In VLSI design, which process deals with the determination of resistance & capacitance of interconnections?

a. Floor planning
b. Placement & Routing
c. Testing
d. Extraction

18) In VHDL, which object/s is/are used to connect entities together for the model formation?

a. Constant
b. Variable
c. Signal
d. All of the above

19) Which data type in VHDL is non synthesizable & allows the designer to model the objects of dynamic nature?

a. Scalar
b. Access
c. Composite
d. File

20) Which type of simulation mode is used to check the timing performance of a design?

a. Behavioural
b. Switch-level
c. Transistor-level
d. Gate-level

Course Coordinator

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

HoD

UNNAMALAI INSTITUTE OFTECHNOLOGY

SubaNagar,Kovilpatti–628502

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

An ISO 9001:2015Certified Institution

Department of Computer Science and Engineering

VCSE2201 Designing of Digital System Using VHDL

Assessment Question and Answer

Name : S. Neha

Register No : 953319104019

Year/Department : IV / CSE

No of Question: 20	Mark: 20	Duration: 30mins

1) What is the full form of EDA in terms of VHDL?

A. Electronic Design Automation ✓

B. Electrical Data Automation

C. Electronic Data Auto-collection

D. Electrical Design Adapter

20/20

2) The act of building a model or representation of a digital circuit or system in order to forecast its behaviour and evaluate its usefulness is known as ____.

A. Implementation

B. Simulation ✓

C. Verification

D. Synthesis

3) The process of validating that a digital design satisfies its functional a and performance criteria is referred to as ____.

A. Implementation

B. Simulation

C. Verification ✓

D. Synthesis

4)The process of converting a high-level hardware description language (HDL) design, such as VHDL, into a lower-level representation, often a gate-level netlist, is known as ____.

A. Implementation

B. Simulation

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

C. Verification

D. Synthesis

5) Port name in VHDL is

A. Case sensitive

B. Case insensitive

6) VHDL code is converted into a gate-level representation or netlist by which of the following tools?

A. Verification tools

B. Place and route tools

C. Time analysis tools

D. Synthesis tools

7) Which of the following is not an example of a synthesis tool?

A. Yosys

B. Cadence Genus

C. Prime time

D. Xilinx Vivado HLS

8)Is there any visual or graphical information in a net list file?

A. Yes

B. No

9) Does HDLs emphasize the concept of abstraction?

A. Yes

B. No

10) An HDL takes which of the following approaches?

A. Structure and behavioural approach

B. Object-oriented approach

C. Master-servant approach

11) Verilog enables which modelling techniques?

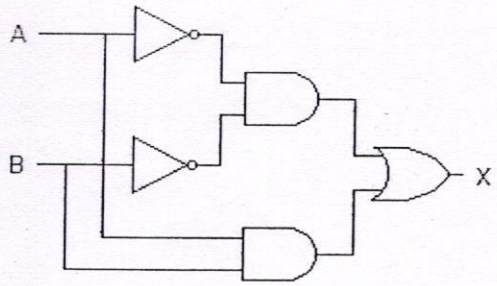
A. Structural modelling techniques

B. Behavioural modelling techniques

C. Both

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

12) What type of logic circuit is represented by the figure shown below?



a) XOR

b) XNOR

c) AND

d) XAND

13) Which of the following combinations of logic gates can decode binary 1101?

a) One 4-input AND gate

b) One 4-input AND gate, one inverter

c) One 4-input AND gate, one OR gate

d) One 4-input NAND gate, one inverter

14) What is the indication of a short to ground in the output of a driving gate?

a) Only the output of the defective gate is affected

b) There is a signal loss to all load gates

c) The node may be stuck in either the HIGH or the LOW state

d) The affected node will be stuck in the HIGH state

14) The carry propagation can be expressed as _____

a) Cp = AB

b) Cp = A + B

c) All but Y0 are LOW

d) All but Y0 are HIGH

15) 3 bits full adder contains _____

a) 3 combinational inputs

b) 4 combinational inputs

c) 6 combinational inputs

d) 8 combinational inputs

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

16) Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?

a. Simulation

b. Optimization

c. Synthesis

d. Verification

17) In VLSI design, which process deals with the determination of resistance & capacitance of interconnections?

a. Floor planning

b. Placement & Routing

c. Testing

d. Extraction

18)In VHDL, which object/s is/are used to connect entities together for the model formation?

a. Constant

b. Variable

c. Signal

d. All of the above

19) Which data type in VHDL is non synthesizable & allows the designer to model the objects of dynamic nature?

a. Scalar

b. Access

c. Composite

d. File

20) Which type of simulation mode is used to check the timing performance of a design?

a. Behavioural

b. Switch-level

c. Transistor-level

d. Gate-leve

Course Coordinator **HoD**

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

UNNAMALAI INSTITUTE OF TECHNOLOGY

Suba Nagar, Kovilpatti–628502

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

An ISO 9001:2015 Certified Institution

Academic Year (2022-2023)

Department of Computer Science and Engineering

VCSE2201 Designing of Digital System Using VHDL

IV Year CSE

S.No	Register Number	Student Name	Maximum Marks	Marks Obtained	Percentage
1	953319104001	Abirami S	20	20	100
2	953319104004	Ajithjkumar A	20	19	95
3	953319104007	Johnebrayeem A J	20	20	100
4	953319104010	Maha Preethi D	20	20	100
5	953319104011	Maheshwari K	20	18	90
6	953319104014	Mathesh Kumar S	20	19	95
7	953319104015	Mesack K	20	20	100
8	953319104017	Muthulakshmi K	20	20	100
9	953319104019	Neha S	20	20	100
10	953319104023	Prasanna Selvi M	20	18	90
11	953319104024	Pushparaj M	20	19	95
12	953319104025	Ragavi K	20	20	100
13	953319104026	Rajkumar C	20	19	95
14	953319104027	Sakthi Kiran K	20	20	100
15	953319104028	Sobiya A	20	20	100
16	953319104029	Sonia D	20	20	100
17	953319104030	Sugan A	20	19	95
18	953319104031	Suriya K	20	20	100
19	953319104032	Ushalakshmi V	20	20	100
20	953319104033	Yalini J	20	19	95

Course Coordinator **HoD**

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

UNNAMALAI INSTITUTE OF TECHNOLOGY

Suba Nagar, Kovilpatti–628502

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

An ISO 9001:2015 Certified Institution

DEPARTMENT OF COMPUTER SCIENCE ENGINEERING

VALUE ADDED COURSE

This is to certify that ABIRAMI S (953319104001 - IV CSE) has participated and successfully completed the 30 hours Value Added Course on VCSE2201 - DESIGNING OF DIGITAL SYSTEM USING VHDL with 100% which was conducted during 22/9/22 to 28/9/22.

at Unnamalai Institute of Technology, Kovilpatti.

Dr. D. RAVINDRAN, M.E., Ph.D.,
Principal
Unnamalai Institute of Technology
Suba Nagar, KOVILPATTI - 628 502.
Thoothukudi District

COURSE COORDINATOR | RESOURCE PERSON | HOD | PRINCIPAL